REMARKS

Status of the Claims

Claims 22-37 are pending, with Claims 22, 38, and 39 being independent. Claim 22 has been amended to recite that the high dielectric constant layer is formed on the interfacial layer. Claims 38 and 39 have been amended to incorporate the recitations of Claim 22, from which Claims 38 and 39 depended. Accordingly, the scope of Claims 38 and 39 has not been narrowed, since the only change made was to make Claims 38 and 39 independent claims, rather than dependent claims. Support for the amendments can be found throughout the specification and within the original claims. Therefore, no new matter has been added.

Applicant respectfully requests the Examiner to reconsider and withdraw the outstanding rejections in view of the foregoing amendments and following remarks.

Claim Rejections Under 35 U.S.C. § 103(a)

Claims 22-40 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over U.S. Patent No. 5,292,673 ("Shinriki") and further in view of U.S. Patent No. 6,087,238 ("Gardner") and U.S. Patent No. 5,322,809 ("Moslehi"). Applicant respectfully disagrees with the rejection; therefore, this rejection is traversed.

Shinriki is cited as disclosing an interfacial layer on a silicon semiconductor substrate; a high dielectric constant layer that comprises a material that is selected from the group consisting of Ta_2O_5, $Ta_2(O_{1-x}N_x)_5$, a solid solution of $(Ta_2O_5)_r$–$(TiO_2)_{1-r}$, a solid

solution of $(Ta_2O_5)_s$–$(Al_2O_3)_{1-s}$, a solid solution of $(Ta_2O_5)_t$–$(ZrO_2)_{1-t}$, and a solid solution of $(Ta_2O_5)_u$–$(HfO_2)_{1-u}$, on the interfacial layer; a gate electrode of an electrically conductive material on the high dielectric constant layer; source and drain regions that are adjacent he gate electrode; and a pair of spacers formed adjacent to the gate electrode and formed on the high dielectric constant layer. Gardner is cited as disclosing a gate of width less than 0.3 microns. Moslehi is cited as disclosing an interlayer insulator that is planar and silicide on source and drain regions.

The Office Action alleges that it would have been obvious to one of ordinary skill in the art at the time of the invention to combine Gardner with Shinriki, because Gardner discloses what the minimum resolution of photolithography is whereas Shinriki is silent on this issue. The Office Action further alleges that it would have been obvious to one of ordinary skill in the art at the time of the invention to combine Moslehi with Shinriki, because the silicide on the source and drain provides for a lower resistivity for better electrical conduction for metal contact and the planar insulator keeps topography level so preceding layers can be uniform. The Office Action additionally alleges that as Applicant has not disclosed that when used in a device, the claimed various high dielectric compositions or interfacial layer materials provide unique or different results from the other materials listed in the group, such as the Ta_2O_5 (high dielectric) or silicon oxide (interfacial layer) disclosed in Shinriki, the claimed materials that are not shown by the prior art of record do not provide patentable distinction from the materials given in the prior art of record.

Shinriki relates to a method of manufacturing a MOSFET using a film of transition metal oxide, such as a tantalum pentoxide film, as a gate insulating film. (Column 1, Lines 10-14). Shinriki discloses forming a silicon oxide layer between a tantalum pentoxide layer and a semiconductor substrate by forming the tantalum pentoxide layer on the semiconductor substrate and, subsequently, applying a heat treatment to the semiconductor substrate in a dry oxidizing atmosphere. (Examples 1, 2, and 5; Claims 1, 25, and 39). As disclosed in the present application, it is believed that the device of Shinriki (wherein a high dielectric constant layer is formed on a substrate rather than on an interfacial layer) has defects including non-uniformity and suffers from high leakage currents, because the silicon oxide layer is formed by reoxidation between the tantalum pentoxide gate insulating film and the silicon substrate. (Page 1, Line 16 – Page 2, Line 2).

Gardner discloses a semiconductor device having a reduced polysilicon gate electrode width along with a process for manufacturing such a device. (Abstract).

Moslehi discloses a self-aligned silicide process that enables different silicide thicknesses for polysilicon gates and source/drain junction regions. (Abstract).

In contrast, Claim 22 recites an MOS transistor formed on a semiconductor substrate of a first conductivity type comprising: (a) an interfacial layer formed on the substrate; (b) a high dielectric constant layer formed on the interfacial layer that comprises a material that is selected from the group consisting of Ta_2O_5, $Ta_2(O_{1-x}N_x)_5$ wherein x ranges from greater than 0 to 0.6, a solid solution of $(Ta_2O_5)_r$-$(TiO_2)_{1-r}$ wherein r ranges from about 0.9 to less than 1, a solid solution $(Ta_2O_5)_s$-$(Al_2O_3)_{1-s}$ wherein s ranges from 0.9

to less than 1, a solid solution of $(Ta_2O_5)_t$-$(ZrO_2)_{1-t}$ wherein t ranges from about 0.9 to less than 1, a solid solution of $(Ta_2O_5)_u$-$(HfO_2)_{1-u}$ wherein u ranges from about 0.9 to less than 1, and mixtures thereof wherein the interfacial layer separates the high dielectric constant layer from the substrate; (c) a gate electrode having a width of less than 0.3 micron covering the high dielectric constant layer; (d) first and second lightly doped regions of a second conductivity type disposed on respective areas of the substrate surface; (e) a source and drain regions of a second conductivity type; and (f) a pair of spacers formed adjacent to the gate electrode and formed on the high dielectric constant layer.

Basic Requirements of a *Prima Facie* Case of Obviousness

As explained in MPEP § 2143, to establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to combine the reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations.

Applicant respectfully submits that neither Shinriki and Gardner nor Shinriki and Moslehi teaches or suggests all the claim limitations. In particular, Applicant respectfully submits that the combination of Shinriki, disclosing a method of manufacturing a MOSFET comprising forming a silicon oxide layer by reoxidation between the tantalum pentoxide gate insulating film and the silicon substrate, is not suggestive of the combination of

features recited in Claim 22, which includes a high dielectric constant layer formed on an interfacial layer. As explained above, the reoxidation heat treatment of Shinriki leads to problems solved by forming a high dielectric constant layer on an already formed interfacial layer.

As the prior art references when combined do not teach or suggest all the claim limitations, a *prima facie* case of obviousness has not been established. Accordingly, withdrawal of the rejection under 35 U.S.C. § 103(a) is respectfully requested.

Discovering Source of a Problem Is Part of "As a Whole" Inquiry

As explained in MPEP § 2141.02, discovery of the source of a problem is part of the 'subject matter as a whole' which should always be considered in determining the obviousness of an invention under 35 U.S.C. § 103." *In re Sponnoble*, 405 F.2d 578, 585, 160 USPQ 237, 243 (CCPA 1969). Applicants who allege they discovered the source of a problem may submit evidence substantiating the allegation, either by way of affidavits or declarations, or by way of a clear and persuasive assertion in the specification. *In re Wiseman*, 596 F.2d 1019, 201 USPQ 658 (CCPA 1979).

As noted above, Shinriki discloses forming a tantalum pentoxide layer on a silicon substrate and later forming a silicon oxide layer between the tantalum pentoxide layer and the semiconductor substrate by applying a heat treatment to the semiconductor substrate in a dry oxidizing atmosphere. As disclosed in the present application, the defects of Shinriki, including non-uniformity and high leakage currents, are believed to be caused by the silicon

oxide layer formed by reoxidation between the tantalum pentoxide gate insulating film and the silicon substrate. The combination of features recited in Claim 22 addresses and solves the problem caused by the reoxidation heat treatment of Shinriki.

Prior Art Disclosures that Teach Away from the Claims Must Be Considered

As further explained in MPEP § 2141.02, a prior art reference must be considered in its entirety, *i.e.*, as a whole, including portions that would lead away from the claimed invention. *W.L. Gore & Associates, Inc. v. Garlock, Inc.*, 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983), *cert. denied*, 469 U.S. 851 (1984).

Again, Shinriki discloses forming a silicon oxide layer between a tantalum pentoxide layer and a semiconductor substrate by forming the tantalum pentoxide layer on the semiconductor substrate and, subsequently, applying a heat treatment to the semiconductor substrate in a dry oxidizing atmosphere. Thus, Shinriki teaches away from the combination of features recited in Claim 22, which recites that the high dielectric constant layer is formed on the interfacial layer.

Legal Concept of *Prima Facie* Obviousness as Applied to Claims 38 and 39

Claim 38 recites an MOS transistor formed on a semiconductor substrate of a first conductivity type comprising: (a) an interfacial layer formed on the substrate, wherein the interfacial layer comprises silicon nitride; (b) a high dielectric constant layer formed on the interfacial layer that comprises a material that is selected from the group consisting of

Ta_2O_5, $Ta_2(O_{1-x}N_x)_5$ wherein x ranges from greater than 0 to 0.6, a solid solution of $(Ta_2O_5)_r$-$(TiO_2)_{1-r}$ wherein r ranges from about 0.9 to less than 1, a solid solution $(Ta_2O_5)_s$-$(Al_2O_3)_{1-s}$ wherein s ranges from 0.9 to less than 1, a solid solution of $(Ta_2O_5)_t$-$(ZrO_2)_{1-t}$ wherein t ranges from about 0.9 to less than 1, a solid solution of $(Ta_2O_5)_u$-$(HfO_2)_{1-u}$ wherein u ranges from about 0.9 to less than 1, and mixtures thereof wherein the interfacial layer separates the high dielectric constant layer from the substrate; (c) a gate electrode having a width of less than 0.3 micron covering the high dielectric constant layer; (d) first and second lightly doped regions of a second conductivity type disposed on respective areas of the substrate surface; (e) a source and drain regions of a second conductivity type; and (f) a pair of spacers formed adjacent to the gate electrode and formed on the high dielectric constant layer.

Claim 39 recites an MOS transistor formed on a semiconductor substrate of a first conductivity type comprising: (a) an interfacial layer formed on the substrate, wherein the interfacial layer comprises silicon oxynitride; (b) a high dielectric constant layer formed on the interfacial layer that comprises a material that is selected from the group consisting of Ta_2O_5, $Ta_2(O_{1-x}N_x)_5$ wherein x ranges from greater than 0 to 0.6, a solid solution of $(Ta_2O_5)_r$-$(TiO_2)_{1-r}$ wherein r ranges from about 0.9 to less than 1, a solid solution $(Ta_2O_5)_s$-$(Al_2O_3)_{1-s}$ wherein s ranges from 0.9 to less than 1, a solid solution of $(Ta_2O_5)_t$-$(ZrO_2)_{1-t}$ wherein t ranges from about 0.9 to less than 1, a solid solution of $(Ta_2O_5)_u$-$(HfO_2)_{1-u}$ wherein u ranges from about 0.9 to less than 1, and mixtures thereof wherein the interfacial layer separates the high dielectric constant layer from the substrate; (c) a gate electrode

having a width of less than 0.3 micron covering the high dielectric constant layer; (d) first and second lightly doped regions of a second conductivity type disposed on respective areas of the substrate surface; (e) a source and drain regions of a second conductivity type; and (f) a pair of spacers formed adjacent to the gate electrode and formed on the high dielectric constant layer.

As explained in MPEP § 2142, "The examiner bears the initial burden of factually supporting any *prima facie* conclusion of obviousness. If the examiner does not produce a *prima facie* case, the applicant is under no obligation to submit evidence of nonobviousness."

As noted above, with regard to Claims 38 and 39, the Office Action concedes that "neither Shinriki, Gardner nor Moslehi disclose the various high dielectric compositions or interfacial layer materials" presently claimed. As such, the Office Action fails to set forth a *prima facie* case of obviousness with regard to Claims 38 and 39. Given the lack of a *prima facie* case of obviousness, there is no justification for the following position taken in the Office Action:

> However, applicant does not disclose these materials to provide unique or different results, when used in a device, from the other materials listed in the group; such as the Ta_2O_5 (high dielectric) or silicon oxide (interfacial layer) disclosed in Shinriki. Therefore the other materials that are not shown by the prior arts of record do not provide patentable distinction from the materials given in the prior arts of record.

Applicant respectfully submits that as the examiner has not met the initial burden of factually supporting any *prima facie* conclusion of obviousness, the applicant is under no obligation to submit evidence of nonobviousness.

Conclusion

For the reasons noted above, the art of record does not disclose or suggest the inventive concept of the presently claimed invention as defined by the claims.

In view of the foregoing amendments and remarks, reconsideration of the claims and allowance of the subject application is earnestly solicited. The Examiner is invited to contact the undersigned at the below-listed telephone number, if it is believed that prosecution of this application may be assisted thereby.

Respectfully submitted,

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